ABSTRACT OF THE DISCLOSURE

A data bus is provided having both a synchronous clock and a channel of data control information integrated in a single signal path. For a data bus having a particular bit time, the integrated clock and control signal has clock high and low time in units equal to one bit time. One edge of the integrated clock and control signal is fixed in phase for bit timing; the alternate edge is phase-modulated. The phase-modulated clock edge carries framing and control data. The fixed-phase bit-timing edge regulates a DLL or PLL to extend the timing. The clock rate is preferably chosen to be equal to the multiplexing cycle rate of multiplexed data carried on the parallel bus.